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Murthi Nanja

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EXAMINER

DAO, THUY CHAN

ART UNIT

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PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

### Office Action Summary

**Application No.**

10/659,457

**Applicant(s)**

NANJA ET AL

**Examiner**

Thuy Dao

**Art Unit**

2192

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 08 October 2008.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1,3-17 and 19-30 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,3-17 and 19-30 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 10 September 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB08)
- 4) ☐ Interview Summary (PTO-413)
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_
- Paper No(s)/Mail Date \_\_\_\_\_

#### **DETAILED ACTION**

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114.

Applicant's submission filed on October 8, 2008 has been entered.

2. Claims 1, 3-17, and 19-30 have been examined.

#### **Response to Amendments**

3. In the instant amendment, claims 1, 11, 13, 17, 19, 24, and 28 have been amended.

4. The objection to the specification and claim 10 is withdrawn in view of Applicant's amendments.

#### **Response to Arguments**

5. Applicants' arguments have been considered but are moot in view of the new ground(s) of rejection.

#### **Specification**

6. Claims 17 and 19-27 direct to "An article of manufacture comprising a machine-accessible medium having a plurality of machine assessable instructions...".

The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter "a machine-accessible medium". See 37 CFR 1.75(d)(1) and MPEP § 608.01(o).

Correction is requested to direct "a machine-accessible medium" to a machine-accessible storage medium.

For the purpose of compact prosecution, the examiner treats the phrase as - - An article of manufacture comprising a [[machine-accessible medium]] storage

device having a plurality of machine assessable instructions...- as disclosed in the specification, page 5, [0020].

### **Claim Rejections – 35 USC §102**

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1, 8-10, 12-17, 21-22, and 24-30 are rejected under 35 U.S.C. 102(b) as being anticipated by "Profiled Guided Selection of ARM and Thumb Instructions" to Gupta et al. (art of record, IDS filed October 23, 2006, but not applied in the previous Office action).

#### **Claim 1:**

Gupta discloses *a method of executing a non-native software instruction, the method comprising:*

*receiving the non-native software instruction at a device (e.g., page 56, non-native embedded applications executed using the ARM family of processors, which supports both 16-bit Thumb instruction set and 32-bit ARM instruction set);*

*generating directly compiling the non-native software instruction to generate a first native software instruction from a first instruction set instruction (e.g., page 61, right column, section 5 "Fine grained generation of mixed code", which generates Thumb code for the entire function, i.e., all non-native software instructions of a particular function are compiled to a first native software instructions Thumb, page 62, section 5.2 "Our Approach"),*

*executing the first native software instruction at the device; counting a number of times the first native software instruction is executed; if the number of times the first native software instruction is executed exceeds a threshold, directly*

*compiling the non-native software instruction to generate a second native software instruction from a second instruction set of at file device (e.g., page 61, right column, section 5.1 "Analysis of Instruction Counts", executing and counting; page 62, left column, detecting patterns and replacing them by ARM instruction sequences, wherein the ARM instruction sequences are compiled from non-native embedded applications; page 62, left column, section 5.2 "Our Approach" and page 58, right column, section 4)*

*wherein the second instruction set is different from the first instruction set (e.g., page 56, 32-bit ARM instruction set is different with 16-bit Thumb instruction set); and*

*executing the second native software instruction at the device (e.g., page 63, right column, section 5.4 "Results", Table 10, executing embedded applications in mixed ARM and Thumb code in the ARM processor; page 64, section 6).*

**Claim 8:**

The rejection of claim 1 is incorporated. Gupta discloses *the first native software instruction comprises an X-bit wide instruction, the second native software instruction comprises a Y-bit wide instruction, and X is less than Y* (e.g., page 56, 16-bit Thumb instructions and 32-bit ARM instructions).

**Claim 9:**

The rejection of claim 1 is incorporated. Gupta discloses *the first native software instruction comprises a 16-bit wide instruction, and the second native software instruction comprises a 32-bit wide instruction* (e.g., as above, page 56).

**Claim 10:**

The rejection of claim 1 is incorporated. Gupta discloses *the first native software instruction comprises a Thumb instruction, and the second native software instruction comprises an ARM instruction* (e.g., as above, page 56).

**Claim 12:**

The rejection of claim 1 is incorporated. Gupta further discloses:

*configuring a first code optimization option prior to generation of the first native software instruction, the first code optimization option causing smaller code to be generated (e.g., page 57, left column, Thumb instructions lead to smaller size); and*

*configuring a second code optimization option prior to generation of the second native software instruction, the second code optimization option causing faster code to be generated (e.g., page 57, left column, ARM instructions run faster Thumb instructions).*

**Claim 13:**

The rejection of claim 1 is incorporated. Gupta further discloses:

*compiling the non-native software instruction to generate the first native software instruction comprises generating a first plurality of native software instructions (e.g., page 57, left column, section 2.2 "Thumb Implementation"), and*

*compiling the non-native software instruction to generate a second native software instruction comprises generating a second plurality of native software instructions (e.g., page 57, right column, section 2.3 "ARM vs. Thumb Instruction Sets), the method further comprising:*

*counting a first number of instructions contained within the first plurality of native software instructions; counting a second number of instructions contained within the second plurality of native software instructions (e.g., page 61, right column, section 5.1 "Analysis of Instruction Counts"); and*

*comparing the first number of instructions and the second number of instructions, wherein executing the first native software instruction is in response to one of (i) the second number of instructions equaling the first number of instructions (e.g., page 62, left column, section 5.3 "Patterns") and*

(ii) *the second number of instructions exceeding the first number of instructions* (e.g., page 58, right column, section 4.1 “Heuristics”; page 61, section 5.1 “Analysis of Instruction Counts”).

**Claim 14:**

The rejection of claim 13 is incorporated. Gupta further discloses *comparing the first number of instructions and the second number of instructions, wherein executing the second native software instruction is in response to the first number of instructions not exceeding the second number of instructions by more than a predetermined threshold* (e.g., page 61, calculating Thumb instruction counts and ARM instruction counts).

**Claim 15:**

The rejection of claim 1 is incorporated. Gupta further discloses *measuring the first native software instruction resulting in a first number of bytes; measuring the second native software instruction resulting in a second number of bytes; and comparing the first number of bytes and the second number of bytes, wherein executing the first native software instruction is in response to the first number of bytes being less than the second number of bytes by at least a predetermined threshold* (e.g., page 60, left column, Heuristic III).

**Claim 16:**

The rejection of claim 1 is incorporated. Gupta further discloses *measuring the first native software instruction resulting in a first number of bytes; measuring the second native software instruction resulting in a second number of bytes; and comparing the first number of bytes and the second number of bytes, wherein executing the second native software instruction is in response to the first number of bytes not being less than the second number of bytes by at least a predetermined threshold* (e.g., page 60, left column, Heuristic IV).

**Claims 17, 21-22, and 24-27:**

Claims 17, 21-22, and 24-27 recite the same limitations as those of claims 1, 8-10, and 12-16, wherein all claimed limitations have been addressed and/or set forth above. Therefore, as the references teach all of the limitations of the above claims, they also teach all of the limitations of claims 17, 21-22, 24-27.

**Claim 28:**

Gupta discloses *an apparatus structured to execute a mixed mode code, the apparatus comprising:*

*a memory device; and a mixed mode processor operatively coupled to the memory device, the mixed mode processor being structured to execute a runtime environment, the runtime environment being stored in the memory device (e.g., page 56, non-native embedded applications executed using the ARM family of processors, which supports both 16-bit Thumb instruction set and 32-bit ARM instruction set), the runtime environment comprising:*

*a compiled binary comprising a plurality of non-native instructions (e.g., page 56, non-native embedded applications executed using the ARM family of processors);*

*a first code generator to compile at least one of the non-native instructions to generate a first native software instruction, the first native software instruction being associated with a first instruction set of the mixed mode processor (e.g., page 61, right column, section 5.1 "Analysis of Instruction Counts", executing and counting; page 62, left column, detecting patterns and replacing them by ARM instruction sequences, wherein the ARM instruction sequences are compiled from non-native embedded applications; page 62, left column, section 5.2 "Our Approach" and page 58, right column, section 4),*

*a counter to count a number of times the first software instruction is executed; a second code generator to generate a second software instruction, a second code generator to compile at least one of the non-native instructions to generate a second native software instruction if the number of times the first native*



*software instruction is executed exceeds a threshold (e.g., page 61, right column, section 5.1 "Analysis of Instruction Counts", executing and counting; page 62, left column, detecting patterns and replacing them by ARM instruction sequences, wherein the ARM instruction sequences are compiled from non-native embedded applications; page 62, left column, section 5.2 "Our Approach" and page 58, right column, section 4),*

*the second native software instruction being associated with a second instruction set of the mixed mode processor (e.g., page 56, 32-bit ARM instruction set is different with 16-bit Thumb instruction set),*

*wherein the first instruction set is different than the second instruction set; and an executing code including the first instruction and the second instruction (e.g., page 63, right column, section 5.4 "Results", Table 10, executing embedded applications in mixed ARM and Thumb code in the ARM processor; page 64, section 6).*

**Claims 29-30:**

Claims 29-30 recite the same limitations as those of claims 8-9, wherein all claimed limitations have been addressed and/or set forth above. Therefore, as the references teach all of the limitations of the above claims, they also teach all of the limitations of claims 29-30.

**Claim Rejections – 35 USC §103**

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

11. Claims 3 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gupta in view of US Patent No. 6,170,083 to Adl-Tabatabai et al. (art made of record, hereafter "Adl-Tabatabai").

**Claim 3:**

The rejection of claim 1 is incorporated. Gupta does not explicitly disclose *inserting instrumentation to count the number of times the first native software instruction is executed*.

However, in an analogous art, Adl-Tabatabai further discloses *inserting instrumentation to count the number of times the first native software instruction is executed* (e.g., FIG. 4, block 450 and related text).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine Adl-Tabatabai's teaching into Gupta's teaching. One would have been motivated to do so to detect hot execution path and optimize accordingly as suggested by Adl-Tabatabai (e.g., col.1: 49 – col.2: 6).

**Claim 19:**

Claim 19 recites the same limitations as those of claim 3, wherein all claimed limitations have been addressed and/or set forth above. Therefore, as the references teach all of the limitations of the above claim, they also teach all of the limitations of claim 19.

12. Claims 4-7, 11, 20, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gupta in view of US Patent Publication No. 2003/0217248 A1 to Nohl al. (art made of record, hereafter "Nohl").

**Claim 4:**

The rejection of claim 1 is incorporated. Gupta does not explicitly disclose *receiving the threshold via a mobile runtime configuration parameter*.

However, in an analogous art, Nohl further discloses *receiving the threshold via a mobile runtime configuration parameter* (e.g., [0003]-[0010], [0018]-[0021]).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine Nohl's teaching into Gupta's teaching. One would have been motivated to do so to optimize runtime dynamic code as suggested by Nohl (e.g., [0015]-[0020]).

**Claim 5:**

The rejection of claim 1 is incorporated. Nohl discloses *receiving the non-native software instruction at the device comprises receiving an intermediate language instruction at the device* (e.g., [0036]-[0041], [0070]-[0073]).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine Nohl's teaching into Gupta's teaching. One would have been motivated to do so as set forth above.

**Claim 6:**

The rejection of claim 1 is incorporated. Nohl discloses *receiving the non-native software instruction at the device comprises receiving Java byte code at the device* (e.g., [0019], [0032], [0040]-[0044]).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine Nohl's teaching into Gupta's teaching. One would have been motivated to do so as set forth above.

**Claim 7:**

The rejection of claim 1 is incorporated. Nohl further discloses *receiving the non-native software instruction at the device comprises wirelessly receiving the non-native software instruction at a hand-held computing device* (e.g., [0008]-[0010], [0082]).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine Nohl's teaching into Gupta's teaching. One would have been motivated to do so as set forth above.

**Claim 11:**

The rejection of claim 1 is incorporated. Nohl discloses *compiling the non-native software instruction at the device comprises using a just-in-time compiler* (e.g., [0019], [0036]-[0041]).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine Nohl's teaching into Gupta's teaching. One would have been motivated to do so as set forth above.

**Claims 20 and 23:**

Claims 20 and 23 recite the same limitations as those of claims 4-7 and 11, wherein all claimed limitations have been addressed and/or set forth above. Therefore, as the references teach all of the limitations of the above claims, they also teach all of the limitations of claims 20 and 23.

**Conclusion**

13. . The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

US Patent No. 6,345,384 discloses selecting most effective instruction sets (FIG. 21) based on either code size or clock cycles (FIG. 27-28).

US Patent No. 7,356,673 discloses compilers targeting two instruction sets such as ARM and THUMB based on most frequently executed code blocks (col.5: 6-24).

14. Any inquiry concerning this communication should be directed to examiner Thuy Dao (Twee), whose telephone/fax numbers are (571) 272 8570 and (571) 273 8570, respectively. The examiner can normally be reached on every Tuesday, Thursday, and Friday from 6:00AM to 6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam, can be reached at (571) 272 3695.

The fax phone number for the organization where this application or proceeding is assigned is (571) 273 8300.

Any inquiry of a general nature of relating to the status of this application or proceeding should be directed to the TC 2100 Group receptionist whose telephone number is (571) 272 2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Thuy Dao/  
Examiner, Art Unit 2192

/Tuan Q. Dam/  
Supervisory Patent Examiner, Art Unit 2192